On-Chip Thermal Management of Nanoelectronic Hot Spots

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InterPack Tutorial
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Portland, OR
On Chip Thermal Management of Nanoelectronic Hot Spots

- History of Thermal Packaging
- On-Chip Hot Spots
- On-Chip Cooling Options
  - Conductive, Convective/Ebullient, Thermoelectric
- On-Chip Thermoelectric Coolers
  - Superlattice, Mini-Contact, Self-Cooling
- Summary
Electronic Numerical Integrator and Computer
ENIAC (1946)
**History of Thermal Packaging**

“The Inward Migration”- an Uncompleted Journey

- **Air Cooling Era: 1965-1980**
  - ENIAC, IBM Mainframes/Telephone switching equipment
  - Vacuum tubes and early solid-state transistors
  - **Goal:** Remove heated air from room/rack/cabinet

- **Liquid/Refrigerant Cooling Era: 1975-1990**
  - Maturation of bipolar devices: ~5W Chips, ~5kW racks
  - Honeywell, IBM, CDC, Hitachi, NEX, Fujitsu mainframes/supers
  - **Goal:** Gain control over the local “heat sink” temperature

- **Enhanced Air Cooling Era: 1985-2000**
  - Thermally-engineered heat sinks for CMOS microprocessors
  - Miniaturized servers create Data Center cooling challenge
  - **Goals:**
    - Reduce “case-to-air” resistance for chip package
    - Improve Data Center thermal management
IBM Air-Cooled Mainframes – 1950’s/1960’s

IBM Mark I Mainframe (1950's)

IBM System 360; SLT Chips: 1964

7/26/2011
CDC Refrigerated Computers 7600 + Cyber 201/203 1971-1983

- Pioneering refrigeration cooled mainframe
- Refrigerant channels under large PCB’s, later Water cooled PCB’s
IBM Water-Cooling Technology 1985

IBM TCM Module

IBM 3081
Air-Cooled Electronic Systems ~ 1990

- 8CPU
- 470x580x80
- 1600W
- Airflow ~ 3.5 m/s

- DC-DC Converter
- System control LSI
- Memory

Air flow
Heat Conduction - BGA Package

Schematic of BGA Package

- Au Wire
- Encapsulation (Mold)
- Silicon Die
- Large Eutectic Solder Balls for High Reliability
- Easy/inexpensive to use 1.0 mm BGA Pitch
- Proven Rigid Substrate Interposer Technology
Thermal Packaging Morphology

- Heat Generation – Nano scale
- Heat Spreading – Micro scale
- Heat Transport – Meso scale
- Heat Rejection – Macro scale

Diagram showing a CPU/heat sink and a fan, indicating the pathways of heat transfer.
Microchannel Cold Plates

Closed Liquid Loop Prototype – to Liquid

Server cold plates mate with liquid cooled cold plates on Rack
Chip Power/Heat Flux Trends (iNEMI’06)

Servers

Max. Steady-State Chip Power (W)
Max. Chip Heat Flux (W/cm²)
Chip Area (cm²)

Desk Top PC's

Max Chip Power (W)

Automotive

Max Chip Power (W)
Max Chip Heat Flux (W/cm²)
Chip Area (cm²)
## 3D Packaging Configurations

<table>
<thead>
<tr>
<th>Technology &amp; z-Interconnect</th>
<th>Module</th>
<th>Application</th>
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</thead>
<tbody>
<tr>
<td><strong>Die Stacking (ChipPAC)</strong></td>
<td>![Die Stacking Image]</td>
<td>Memory</td>
</tr>
<tr>
<td>Wire Bond</td>
<td>![Wire Bond Image]</td>
<td>Memory + ASIC + Memory</td>
</tr>
<tr>
<td><strong>Package Stacking (ChipPAC)</strong></td>
<td>![Package Stacking Image]</td>
<td>Memory</td>
</tr>
<tr>
<td>Wire Bond</td>
<td>![Wire Bond Image]</td>
<td>Memory + ASIC + Memory</td>
</tr>
<tr>
<td><strong>Die Stacking (ChipPAC)</strong></td>
<td>![Die Stacking Image]</td>
<td>ASIC + other</td>
</tr>
<tr>
<td>Flip Chip</td>
<td>![Flip Chip Image]</td>
<td></td>
</tr>
<tr>
<td><strong>Package Stacking (Amkor)</strong></td>
<td>![Package Stacking Image]</td>
<td>Memory</td>
</tr>
<tr>
<td>Solder Ball</td>
<td>![Solder Ball Image]</td>
<td></td>
</tr>
<tr>
<td><strong>Folded Stacking (Tessera)</strong></td>
<td>![Folded Stacking Image]</td>
<td>Memory</td>
</tr>
<tr>
<td>Substrate + Solder Ball</td>
<td>![Substrate + Solder Ball Image]</td>
<td>Memory + ASIC + Memory</td>
</tr>
</tbody>
</table>

(Dereje Agonafer and Bahgat Sammakia, InterPACK'05)
On-Chip mP Power/Temperature (Watwe/Prasher, IMECE’01)
Analytical Calculation of Hot Spot

$$\Delta T_{\text{hotspot}} = \frac{q_{\text{hotspot}}}{k_{\text{Si}}} \left( - \frac{0.233}{r_{\text{hotspot}}} - 2094w_{\text{hotspot}}^2 + 0.56w_{\text{hotspot}} \right)$$

$$\Delta T_{\text{semi-infinite}} = \frac{q_{\text{hotspot}} W_{\text{hotspot}}}{\pi^{0.5} k_{\text{Si}}}$$

Exact Sol.     Simplified Sol.

- 100µm
- 200µm
- 300µm
- 400µm
- 500µm

Semi-infinite

Hot Spot Flux: 1000W/cm²
2000- Thermal Packaging “Triple Threat”

Nanoelectronics Era: 2000 -
GHz-level CMOS with features below 100 nanometers
Distinct on-chip “hot spots” - silicon/compound semiconductors
Emergence of homogeneous/heterogeneous “chip stacks”
Goals:
Reduce/eliminate on-chip “hot spots”
Overcome internal “stack” resistance
On Chip Thermal Management of Nanoelectronic Hot Spots

- History of Thermal Packaging
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Thermal Packaging Challenge
Microprocessor Hot Spots (IBM, 2008)


q” hot spot = 500W/cm², 2x2mm; q” avg = 50W/cm², 40x40mm
High Heat Flux GaN-Based RF Components

Thermal Simulation of GaN MMIC SiC die (380 μm thick) attached to 2-part (closed channel) copper cooler with 50 μm of Sn-3.5Ag

Calame, et al., IEEE Transactions on Components and Packaging Technologies, Vol. 28 Issue 4, pp. 797-809, 2005

7/26/2011
Multiple Hot Spots on GaN MMIC Die

GaN temperature (°C)

![Graph showing temperature distribution across the GaN MMIC Die](image)

Morag Garven, IEEE TRANSACTIONS ON COMPONENTS AND PACKAGING TECHNOLOGIES, VOL. 32, NO. 1, MARCH 2009
Nano Transistor Temperature Field

MOSFET device; Gate length = 90 nm
volumetric power dissipation = 5W/um3 over a radius of 20 nm
(Sinha and Goodson, Therminic 2004)
Multiple Hot Spots on IGBT Module

1. Toyota 2004 Prius motor inverter module;
2. 12 pairs of IGBT and diode with a total power dissipation of 2400W on the inverter module;
3. Power density of IGBT is 120W/cm² and diode is 95 W/cm².

Multiple Hot Spots on IGBT Module

Toyota Prius Motor Inverter Module with Single-Phase Cooling Cold Plate

(A) Pumping Power: 0.3W

(B) Pumping Power: 0.5W

(C) Pumping Power: 1.0W

(D) Pumping Power: 4.0W
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TIM Effective Thermal Resistance

\[ R_{TIM} = R_{c_1} + \frac{BLT}{k_{TIM} A} + R_{c_2} \]
Thermal Interface Technologies

(Viswanath et al., 2000)
Orthotropic Spreader
Excess Temperature Profiles

"Radial\Delta T_{\text{bulk}}\text{ on chip bottom for different in-plane conductivities}"

- Isotropic
  - $k_{xy} = 350\text{ W/m-K}$
- 9.3 K Reduction
- 14.3 K Reduction
- $k_{xy} = 1800\text{ W/m-K}$

$k_{z} = 5\text{ W/m-K}$
$q'' = 1.4\text{ kW/cm^2}$
hotspot size = 500 um
$h = 10,000\text{ W/m^2-K}$
$T_{\text{bulk}} = 298\text{ K}$

ECTC 2011
ABC/KJLG Thermal Management
Hot Spot on GaN-SiC Package

Hot Spot on GaN-SiC (2D Representation)

Hot Spot Cooling on GaN-SiC

Note: $\Theta_{\text{tot}} = T_{\text{max}} - T_{\text{amb}}$
3D Thermal Interconnect

(Balandin, 2009)
Example Heat Pipe Assemblies
(www.aavidthermalloy.com)
Custom/Military Applications
ISR Spraycool™ Technology

ABC/KJLG Hot Spots & 3D
Spray Evaporative Cooling
Cray 3 Design

(Cray-3)
Cooling 3D Chips with Water Flow Networks

The complexity of such a system resembles that of a human brain, wherein millions of nerves and neurons for signal transmissions are intermixed but do not interfere with tens of thousands of blood vessels for cooling and energy supply, all within the same...
Thermoelectric Hot Spot Cooling

Without TE Cooler:
- $q=100\,W$
- $T_A=25^\circ C$
- $R_{HS}=0.55\,K/W$
- $R_{TIM}=0.04\,K/W$
- $R_{die}=0.048\,K/W$
- $q=98\,W$
- $R_{die}=7.42\,K/W$
- $T_{chip}=89^\circ C$
- $T_{Hot\text{-}spot}=104^\circ C$
- $q=2\,W$

With TE Cooler:
- $q=98\,W+2\,W+5\,W$
- $T_A=25^\circ C$
- $R_{HS}=0.55\,K/W$
- $R_{TIM}=0.04\,K/W$
- $R_{die}=0.048\,K/W$
- $q=98\,W$
- $R_{die}=7.42\,K/W$
- $T_h=92^\circ C$
- $T_{chip}=89^\circ C$

TE Cooler:
- COP=0.4; $\Delta T=-23K$

$THOT\text{-}SPOT=84^\circ C$

ABC/KJLG Hot Spots & 3D

ECTC 2010
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**Principle of Thermoelectric Cooler**

**Thermoelectric Cooler (TEC)** is a solid-state device that can pump the heat from one side of the device to the other side when an electric current is applied.

**Advantages of Micro-TEC**
- Spot cooling ability
- No moving parts
- High reliability
- High cooling power density
- Compact structure
- Small volume and low weight

![Diagram of Thermoelectric Cooler](image)

Net Cooling Power on Silicon Chip

\[ Q_{cooling} = -STcI + \frac{1}{2}I^2R_{elec} + \frac{T_h - T_c}{R_{th}} \]
Superlattice TEC for Hot Spot Cooling

400μm× 400μm Hot Spot, 1250W/cm² Heat Flux

Intel and Nextreme Thermal Solutions

Superlattice TEC for Hot Spot Cooling
Superlattice Micro-TEC Fabrication

[Diagram of Superlattice Micro-TEC Fabrication]

- A: GaAs substrate, n-superlattice, p-superlattice, Contact metallization
- B: Sacrificial substrate, Electroplated Cu, Solder
- C: IHS, Cu traces on IHS, Dielectric
- D: Heat absorption, PWR, GND, Heat rejection
- E: Thermoelectric cooler, Integrated Heat Spreader (IHS)
Hot Spot Cooling Performance

Baseline - no TEC

Passive cooling (7.6 °C)

On-demand cooling swing (7.3 °C)
Mini-Contact TEC for Hot Spot Cooling

$400\mu m \times 400\mu m$ Hot Spot, $1250W/cm^2$ Heat Flux

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Mini-Contact TEC Concept
# Geometry, Materials Properties

<table>
<thead>
<tr>
<th>Geometry (L × W × H)</th>
<th>Material</th>
<th>K (W/mK)</th>
<th>Boundary Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heat Sink Base</td>
<td>Al</td>
<td>180</td>
<td>$h_{\text{eff}} = 0.072,\text{W/cm}^2\text{K}$</td>
</tr>
<tr>
<td>IHS</td>
<td>Cu</td>
<td>360</td>
<td></td>
</tr>
<tr>
<td>TIM3</td>
<td>/</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>TIM2</td>
<td>/</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>Top ceramic</td>
<td>AIN</td>
<td>180</td>
<td></td>
</tr>
<tr>
<td>TEC element*</td>
<td>Bi$_2$Te$_3$</td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>TIM1</td>
<td>/</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>Bottom ceramic</td>
<td>AIN</td>
<td>180</td>
<td></td>
</tr>
<tr>
<td>Mini-contact base</td>
<td>Cu</td>
<td>360</td>
<td></td>
</tr>
<tr>
<td>Mini-contact tip</td>
<td>Cu</td>
<td>360</td>
<td></td>
</tr>
<tr>
<td><strong>Die</strong></td>
<td>Si</td>
<td>100</td>
<td>$q''_{bg} = 70,\text{W/cm}^2$</td>
</tr>
<tr>
<td><strong>Hot Spot</strong></td>
<td>/</td>
<td>/</td>
<td>$q''_{hotspot} = 1250,\text{W/cm}^2$</td>
</tr>
</tbody>
</table>

* $S = 200\mu\text{V/K}, \rho = 10\mu\Omega\text{m}$ for Bi$_2$Te$_3$ at room temperature. Electric contact resistance is assumed to be $1 \times 10^{-7} \Omega\text{cm}^2$. 
Temperature Profile on the Silicon Chip

Temperature Profile on the Silicon Chip

Temperature (°C) vs. Position on the Bottom of the Die (µm)

- 137°C
- 128°C
- 125°C
- 120°C

- No TEC & no hotspot
- No TEC & with hotspot
- 600µm mini-contact tip
- 1250µm mini-contact tip
- 2400µm mini-contact tip

20µm thick Bi₂Te₃ element, 500µm thick die, Pᵢᵣₑᵦ = 10W, Rₑᵡ₁ = Rₑᵡ₂ = 1 x 10⁻⁷ m²K/W
Hot Spot Temperature vs. Input Power on TEC

20μm thick Bi₂Te₃ element
1250μmx1250μm Mini-contact tip
500μm thick die
R₁=R₂=1x10⁻⁷ m²K/W
Thermal Contact Resistance Effect

Two Important Thermal Contact Resistance

- $R_{c,1}$: Thermal contact resistance at ceramic/TIM2 interface
- $R_{c,2}$: Thermal contact resistance at mini-contact/silicon die

Typical Values of Thermal Contact Resistance

- $1 \times 10^{-5} \text{ m}^2\text{K/W}$ between thermal grease and metal (ceramics)
- $\sim 1 \times 10^{-7} \text{ m}^2\text{K/W}$ for thin film grown on metal (ceramics)
Thermal Contact Resistance Effect

Case (I) $R_{c1} = R_{c2} = R_c$

![Graph showing the relationship between Hot Spot Temperature (°C) and Mini-Contact Tip Size (μm) with varying $R_c$ values.](image)

- **Hot Spot Temperature (°C)**
  - 160
  - 155
  - 150
  - 145
  - 140
  - 135
  - 130
  - 125
  - 120
  - 115

- **Mini-Contact Tip Size (μm)**
  - 400
  - 600
  - 800
  - 1000
  - 1200
  - 1400
  - 1600
  - 1800
  - 2000
  - 2200
  - 2400
  - 2600

- **$R_c$ (m²K/W)**
  - $1 \times 10^{-7}$
  - $1 \times 10^{-6}$
  - $5 \times 10^{-6}$
  - $1 \times 10^{-5}$

- **Notes**
  - 20 μm thick Bi₂Te₃ element, 500 μm thick die, I=I_{opt}
  - No TEC
Thermoelectric Element Thickness Effect

Graph showing the effect of thermoelectric element thickness on max. hotspot cooling. The x-axis represents the mini-contact tip size (μm), and the y-axis represents the max. hotspot cooling (°C). Three different thicknesses are shown: 100 μm, 50 μm, and 20 μm.

Legend:
- t<sub>TE</sub> = 100 μm
- t<sub>TE</sub> = 50 μm
- t<sub>TE</sub> = 20 μm

Additional information:
- R<sub>c1</sub> = R<sub>c2</sub> = 1 x 10<sup>-7</sup> m<sup>2</sup>K/W
- 500 μm thick die
Silicon Chip Thickness Effect

**Graphs:**
- **Top Left:**
  - Good Thermal Contact: $R_{c1} = R_{c2} = 1 \times 10^{-7} \, \text{m}^2\text{K/W}$
  - 500$\mu$m Thick Die, $I = I_{\text{opt}}$
  - 20$\mu$m thick Bi$_2$Te$_3$ element
  - 17°C Cooling

- **Bottom Left:**
  - Good Thermal Contact: $R_{c1} = R_{c2} = 1 \times 10^{-7} \, \text{m}^2\text{K/W}$
  - 700$\mu$m Thick Die, $I = I_{\text{opt}}$
  - 20$\mu$m thick Bi$_2$Te$_3$ element
  - 10°C Cooling

- **Top Right:**
  - Bad Thermal Contact: $R_{c1} = R_{c2} = 1 \times 10^{-5} \, \text{m}^2\text{K/W}$
  - 500$\mu$m Thick Die, $I = I_{\text{opt}}$
  - 20$\mu$m thick Bi$_2$Te$_3$ element
  - No TEC

- **Bottom Right:**
  - Bad Thermal Contact: $R_{c1} = R_{c2} = 1 \times 10^{-5} \, \text{m}^2\text{K/W}$
  - 700$\mu$m Thick Die, $I = I_{\text{opt}}$
  - 20$\mu$m thick Bi$_2$Te$_3$ element
  - No TEC
Experimental Validation

- Heat Sink
- Thermal Interface Materials (TIM)
- Heat Spreader
- Heat Spreader
- Dummy Silicon Chip
- Thin-Film Heaters
- Thermal Insulation (fiber glass)
- Thermocouple
- Five Different Mini-Contacts
- Heat Spreader
- TEC
- Silicon Wafer
- Experimental Validation
Experimental Validation

- TEC
- Indium Solder
- Mini-Contact
- Silicon Wafer

Silicon Wafer

Thermion TEC
Experimental Validation

![Graph showing the relationship between spot cooling (K) and input power on TEC (W) for different chip powers (0, 30 W, 67 W). The graph includes a legend for chip power and various data points for each power level.]
Experimental Demonstration

Chip Power
- 67W
- 30W
- 0 W

Max. Spot Cooling (K)

Mini-Contact Tip Size (mm)
Silicon Micro-Cooler for Hot Spot Cooling

70μm × 70μm Hot Spot, 700W/cm² Heat Flux

University of Maryland

Silicon Micro-Cooler Concept

Germanium/Silicon Self-Cooling Concept

\[ Q = S_{Ge} TI + R_c I^2 \]

\[ Q = -S_{Ge} TI + R_c I^2 \]

\[ \nabla^2 T + \frac{q_J}{k} = 0, \quad \nabla^2 V + \frac{\rho}{\varepsilon} = 0 \]

Highly Doped N-type Germanium/Silicon

\[ v_{eff}=8741 \text{ W/m}^2\text{-K} \]

\[ h_{eff}=8741 \text{ W/m}^2\text{-K} \]
Silicon Property Variation with Doping Concentration

$\rho_{Si}$ (\(\mu\Omega\cdot m\)) or $S_{Si}$ (\(\mu V/K\))

$T = 100^\circ C$

$\rho_{Si}$

$S_{Si}$

$P_{Si}$

$P$ (\(\mu W/K^2\))

$N_d$ (cm\(^{-3}\))
Silicon Self Cooling
Doping Concentration Effect

\[ \Delta T_{\text{hotspot, max}} \text{ (°C)} \]

\[ \rho_c \text{ (Ω.cm}^2\text{)} \]
- \[ 1 \times 10^{-4} \]
- \[ 1 \times 10^{-5} \]
- \[ 1 \times 10^{-6} \]
- \[ 1 \times 10^{-7} \]

\[ t_{\text{Si}} = 100 \mu\text{m} \]
\[ l_c = w_c = 600 \mu\text{m} \]

Doping Concentration in Silicon \( N_d \) (cm\(^{-3}\))
Numerical Modeling of On-Chip TE Cooling at Hot Spot

Temperature Profile on the Chip

680W/cm² for 70umx70um Hot Spot, 70W/cm² for Background Dissipation. 0.6A Applied Current, 50um Die thickness and 2x10¹⁹cm⁻³ Doping Concentration
Silicon Self Cooling
Micro-Cooler Size Effect

$\Delta T_{max}$ ($^\circ$C) vs. Microcooler Size ($\mu$m)

- $t_{Si} = 100 \mu$m
- $\rho_c = 1 \times 10^{-6} \Omega \cdot \text{cm}^2$
- $N_d = 2.5 \times 10^{19} \text{cm}^{-3}$
Silicon Self Cooling
Substrate Thickness Effect

\[ \rho_c = 1 \times 10^{-6} \ \Omega \text{cm}^2 \]
\[ N_d = 2.5 \times 10^{19} \ \text{cm}^{-3} \]

\[ \Delta T_{\text{max, hotspot}} (\circC) \]

Microcooler Size (\(\mu m\))

Chip Thickness \(t_{\text{Si}}\)
- 100\(\mu m\)
- 200\(\mu m\)
- 300\(\mu m\)
- 400\(\mu m\)
- 500\(\mu m\)
Silicon Self Cooling

Hot Spot Heat Flux Effect

\[ t_{Si} = 100 \mu m \]
\[ \rho_c = 1 \times 10^{-6} \Omega \cdot cm^2 \]
\[ N_d = 2.5 \times 10^{19} cm^{-3} \]

ΔT_{hotspot,max} (°C)

Hotspot Heat Flux (W/cm\(^2\))

- 100
- 250
- 400
- 550
- 700
- 850
- 1000

Hotspot Size (µm)
Silicon Self Cooling
Hot Spot Heat Flux Effect

Hotspot Heat Flux (W/cm$^2$)
- 100
- 250
- 400
- 550
- 700
- 850
- 1000

$\Delta T^*$ hotspot, max

$\mu m$

$\rho_c = 1 \times 10^{-6} \Omega . cm^2$
$N_d = 2.5 \times 10^{19} cm^{-3}$

$t_{si} = 100 \mu m$

Hot Spot is over-cooled
Hot Spot is partially removed
Germanium Self-Cooling for Hot Spot Thermal Management

70μm × 70μm Hot Spot, 700W/cm² Heat Flux

University of Maryland

Self Cooled Germanium Chip Temperature Profile

Temperature Profile

- No Hot Spot
- With Hot Spot, No TEC
- TEC (I=0.50A)
- TEC (I=1.25A)
- TEC (I=2.00A)

Germanium substrate thickness = 100μm
Temperature/Heat Flux In Germanium

No Self-Cooling (I = 0A)  Self-Cooling (I = 0.8A)

Germanium substrate thickness=100μm
Power Factor Variation With Doping Concentration

Power Factor (μW/mK²) vs. Doping Concentration (cm⁻³)

Silicon

Germanium
Germanium Self Cooling: Micro-Cooler Size Effect

Temperature at Hot Spot (°C) vs. Applied Current (A)

Temperature at Cooler (°C) vs. Applied Current (A)

Temperature Reduction (°C) vs. Cooler Size (μm)

Germanium substrate thickness = 100 μm

at Hot Spot

at Micro Cooler

Germanium substrate thickness = 100 μm
Germanium Self Cooling: Substrate Thickness Effect

Temperature Reduction at Hot Spot (°C) vs. Micro Cooler Size (μm)

- Germanium Thickness
  - □ 100μm
  - ○ 300μm
  - ▲ 500μm

(A)
Germanium Self Cooling: Hot Spot Heat Flux Effect

- No Self-Cooling
- Self-Cooling Activated

Hot Spot Temperature (°C) vs. Hot Spot Heat Flux (W/cm²)

Germanium substrate thickness = 100 μm
Germanium Self Cooling
Hot Spot Heat Flux Effect

\[ \Delta T_{\text{hotspot}}^* > 1 \quad \text{hot spot is over-cooled} \]

\[ \Delta T_{\text{hotspot}}^* < 1 \quad \text{hot spot partially removed} \]

\[
\Delta T_{\text{hotspot}}^* = \frac{T_{\text{hotspot, cooler OFF}} - T_{\text{hotspot, cooler ON}}}{T_{\text{hotspot, cooler OFF}} - T_{\text{hotspot, cooler OFF}}}
\]
Germanium-on-Silicon Composite Self Cooling
Tutorial Summary

- Moore’s Law driving deep into nano territory, creating ~ kW/cm² hot spots on high q” background
- Hot spots driving thermal packaging development
- Hot Spot Remediation Possible with On-Chip TEC’s
  - Superlattice TFTEC’s
  - Mini-Contact with Conventional TEC’s
  - Silicon Self-Cooling Microcoolers
  - Germanium Self-Cooling Microcoolers
- Improved TEC materials, TEC fabrication, thermal interfaces, composites, optimum doping….needed for further improvements


